DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Supplementary Examination – Summer 2022

Course: B. Tech. **Branch :** Electrical Engineering **Semester :IV**

Subject Code & Name: Analog and Digital electronics [BTEEE-406B]

Max Marks: 60 **Date:** **Duration: 3 Hr.**

Instructions to the Students:

1. *All the questions are compulsory.*
2. *The level of question/expected answer as per OBE or the Course Outcome (CO) onwhich the question is based is mentioned in ( ) in front of the question.*
3. *Use of non-programmable scientific calculators is allowed.*
4. *Assume suitable data wherever necessary and mention it clearly.*

		(Level/CO)	Marks
Q. 1	**Solve Any Two of the following.**		
A)	Explain cascading of amplifiers with suitable diagram.	CO1	6
B)	Implement following expression using 8:1 multiplexer $F(A, B, C, D) = \sum m(0, 2, 3, 6, 8, 9, 12, 14)$	CO6	6
C)	Explain frequency response curve in detail	CO1	6
Q.2	**Solve Any Two of the following.**		
A)	Explain block diagram of an OPAMP in detail	CO2	6
B)	Explain different parameters of an OPAMP	CO2	6
C)	Compare TTL and CMOS	CO4	6
Q. 3	**Solve Any One of the following.**		
A)	Perform following operations i) (10111.011) - (10110.110) ii) subtract $(1000)_2$ - (0110 $)_2$ using 2's complement method	CO3	6
B)	Using the rules of Boolean Algebra Simplify the following and implement using basic gates $XY + X\bar{Y}Z + X\bar{Y}\bar{Z} + \bar{X}YZ$	CO3	6
C)	Implement all basic logic gates using NOR Gate.	CO3	6
Q.4	**Solve Any Two of the following.**		
A)	Explain Serial in Serial out shift register with waveforms	CO4	6
B)	Design mod-6 ripple counter	CO4	6
C)	Explain J-K flip flop	CO4	6
Q. 5	**Solve Any One of the following.**		
A)	Minimize the following expression using K-Map method and implement the minimized expression using logic gates $F(A, B, C, D) = \sum m(0,1, 2, 3, 6, 8, 9, 12,13, 14,15) + d(5, 7, 10)$	CO5	6
B)	Compare combinational circuit and sequential circuit	CO5	6
C)	Explain operation of full Subtractor.	CO6	6

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